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Case2: When data is changing within setup time of next falling edge of clock for when I 1, I 4 are not removed ... If inverter I 1, I 4 is included, if data D is changed within , it will reach to input of T 3 only after T time. As rising edge will be at T, so at T time when clock's rising edge will be triggered input D will pass through T 3, thus will be present in output.

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